Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended) An integrated circuit comprising a differential impedance termination circuit, the differential impedance termination circuit comprising:

~~first resistors coupled in series; and~~

~~a first transistor coupled in series with the first resistors; and~~

~~a first memory coupled to a gate of the first transistor that is programmed to effect an impedance of the impedance termination circuit,~~

first and second resistors;

first and second transistors coupled in parallel, wherein drains of the first and second transistors are coupled to a first terminal of the first resistor, and sources of the first and second transistors are coupled to a first terminal of the second resistor;

third and fourth transistors coupled in parallel, wherein drains of the third and fourth transistors are coupled to a second terminal of the first resistor, and sources of the third and fourth transistors are coupled to a second terminal of the second resistor;

a third resistor having a first terminal coupled to the second terminal of the first resistor; and

a fourth resistor having a first terminal coupled to the second terminal of the second resistor,

the impedance termination circuit being coupled between first and second differential pins of the integrated circuit.

Claim 2 (currently amended) The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array that includes programmable logic blocks.

Claim 3 (currently amended) The integrated circuit according to claim 1 wherein ~~the integrated circuit is an application specific integrated circuit~~ wherein gates of the first, second, third, and fourth transistors are controlled by four independent control signals.

Claim 4 (currently amended) The integrated circuit according to claim 1 further comprising:

~~a second transistor;~~

~~a second memory coupled to a gate of the second transistor that is programmed to effect the impedance of the impedance termination circuit; and~~

~~a second resistor coupled in series with the second transistor, the second resistors and the second transistor being coupled in parallel with at least one of the first resistors when the second transistor is ON~~

fifth and sixth transistors coupled in parallel, wherein drains of the fifth and sixth transistors are coupled to a second terminal of the third resistor, and sources of the fifth and sixth transistors are coupled to a second terminal of the fourth resistor.

Claim 5 (currently amended) The integrated circuit according to claim 4 further comprising:

~~a third transistor;~~

~~a third memory coupled to a gate of the third transistor that is programmed to effect the impedance of the impedance termination circuit; and~~

~~a third resistor coupled in series with the third transistor, the third resistor and the third transistor being coupled in parallel with at least one of the first resistors when the third transistor is ON~~

a fifth resistor coupled to the second terminal of the third resistor; and

a sixth resistor coupled to the second terminal of the fourth resistor.

Claim 6 (currently amended) The integrated circuit according to ~~claim 4 further comprising~~:

~~a third transistor coupled in parallel with the second resistor; and~~

~~a third memory coupled to a gate of the third transistor~~

claim 5 further comprising:

seventh and eighth resistors, each having a first terminal coupled to the second terminal of the third resistor; and

ninth and tenth resistors, each having a first terminal coupled to the second terminal of the fourth resistor.

Claim 7 (currently amended) The integrated circuit according to claim ~~1~~ 6 further comprising:

~~a second transistor coupled in parallel with the first transistor; and~~

~~a second memory coupled to a gate of the second transistor that is programmed to effect an impedance of the impedance termination circuit~~

a seventh transistor having a drain coupled to a second terminal of the seventh resistor and a source coupled to a second terminal of the ninth resistor; and

an eighth transistor having a drain coupled to a second terminal of the eighth resistor and a source coupled to a second terminal of the tenth resistor.

Claim 8 (original) The integrated circuit according to claim ~~1 further comprising:~~

~~a second transistor coupled in parallel with one or more of the first resistors;~~

~~a third transistor coupled in parallel with the second transistor;~~

~~a second memory coupled to a gate of the second transistor; and~~

~~a third memory coupled to a gate of the third transistor~~

7 wherein gates of the first, second, third, fourth, fifth, sixth, seventh, and eighth transistors are controlled by eight independent control signals that control an impedance of the impedance termination circuit.

Claims 9-19 (canceled)

Claim 20 (new) An integrated circuit comprising a differential termination circuit, the differential termination circuit comprising:

first and second resistors coupled together in series;

a first transistor having a drain coupled to a first terminal of the first resistor;

a second transistor having a source coupled to the first terminal of the first resistor and a drain coupled to a second terminal of the first resistor and a first terminal of the second resistor;

third and fourth resistors coupled together in series, the third resistor having a first terminal coupled to a source of the first transistor; and

a third transistor having a drain coupled to the first terminal of the third resistor and a source coupled to a second terminal of the third resistor and a first terminal of the fourth resistor,

the differential termination circuit being coupled between first and second differential pins of the integrated circuit.

Claim 21 (new) The integrated circuit according to claim 20 wherein the integrated circuit is a field programmable gate array that includes programmable logic elements.

Claim 22 (new) The integrated circuit according to claim 20 further comprising:

a fourth transistor having a drain coupled to a second terminal of the second resistor and a source coupled to a second terminal of the fourth resistor.

Claim 23 (new) The integrated circuit according to claim 22 further comprising:

a fifth resistor having a first terminal coupled to the second terminal of the second resistor; and

a sixth resistor having a first terminal coupled to the second terminal of the fourth resistor.

Claim 24 (new) The integrated circuit according to claim 23 further comprising:

a fifth transistor having a drain coupled to a second terminal of the fifth resistor and a source coupled to a second terminal of the sixth resistor.

Claim 25 (new) The integrated circuit according to claim 24 further comprising:

a sixth transistor coupled in parallel with the fifth resistor; and

a seventh transistor coupled in parallel with the sixth resistor.

Claim 26 (new) The integrated circuit according to claim 25 further comprising:

a seventh resistor coupled to the second terminal of the second resistor; and

an eighth resistor coupled to the second terminal of the fourth resistor.

Claim 27 (new) The integrated circuit according to claim 25 wherein gates of the first, second, third, fourth, fifth, sixth, and seventh transistors are coupled to seven independent control signals that control an impedance of the differential termination circuit.

Claim 28 (new) An integrated circuit comprising a differential termination circuit that is coupled between first and second differential pins, the differential termination circuit comprising:

first and second resistors;

first and second transistors coupled in parallel, wherein drains of the first and second transistors are coupled to a first terminal of the first resistor, and sources of the first and second transistors are coupled to a first terminal of the second resistor; and

third and fourth transistors coupled in parallel, wherein drains of the third and fourth transistors are coupled to a second terminal of the first resistor, and sources of the third and fourth transistors are coupled to a second terminal of the second resistor,

wherein gates of the first, second, third, and fourth transistors are controlled by four independent control signals that control an impedance of the differential termination circuit.